

**AMENDMENTS TO THE CLAIMS:**

Kindly cancel claims 7-15, without prejudice. Please amend claims 1 and 5, and add new claims 16-19, as shown below.

This listing of claims will replace all prior versions and listings of claims in the Application:

**Claim 1 (currently amended):** A semiconductor device comprising:

a first interconnect pattern[[,]] ;

a first dielectric film covering top and side surfaces of said first interconnect pattern and having therein through-holes[[,]] ;

a second interconnect pattern electrically connected to said first interconnect pattern via said through-holes[[,]] ;

a semiconductor chip having a plurality of chip electrodes ~~and~~ , said chip mounted [[on]] so as to contact said first dielectric film[[,]] ;

interconnect members for connecting said chip electrodes to said second interconnect patterns[[,]] ;

an encapsulating resin for encapsulating said semiconductor chip and said interconnect members on said first dielectric film[[,]] ; and

a second dielectric film covering a bottom surface of said first interconnect pattern.

**Claim 2 (original):** A semiconductor device as defined in claim 1, further comprising a plurality of external terminals formed on said bottom surface of said first interconnect pattern and exposed from said second dielectric film.

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**Claim 3 (original):** The semiconductor device as defined in claim 2, wherein said external terminals are metallic bumps.

**Claim 4 (withdrawn):** The semiconductor device as defined in claim 1, wherein portions of said first interconnect pattern are formed as a plurality of external terminals.

**Claim 5 (currently amended):** The semiconductor device as defined in claim 1, wherein said interconnect members are metallic bumps and one surface of said semiconductor chip is exposed.

**Claim 6 (withdrawn):** The semiconductor device as defined in claim 1, wherein said interconnect members are bonding wires.

**Claims 7-15 (canceled)**

**Claim 16 (new):** A semiconductor device comprising:

a first interconnect pattern;

a first dielectric film covering top and side surfaces of said first interconnect pattern and having therein through-holes;

a second interconnect pattern electrically connected to said first interconnect pattern via said through-holes;

a semiconductor chip having a plurality of chip electrodes and mounted on said first dielectric film;

interconnect members for connecting said chip electrodes to said second interconnect patterns;

an encapsulating resin for encapsulating said semiconductor chip and said interconnect members on said first dielectric film; and

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a second dielectric film covering a bottom surface of said first interconnect pattern,  
wherein said second interconnect pattern is disposed directly in contact with said  
encapsulating resin.

**Claim 17 (new):** A semiconductor device as defined in claim 16, further comprising a  
plurality of external terminals formed on said bottom surface of said first interconnect pattern  
and exposed from said second dielectric film.

**Claim 18 (new):** A semiconductor device as defined in claim 17, wherein said external  
terminals are metallic bumps.

**Claim 19 (new):** A semiconductor device as defined in claim 16, wherein said  
interconnect members are metallic bumps.

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